IN THE CLAIMS:

The following listing of claims will replace all prior versions, and listings, of claims in the application. Please add claim 64 as indicated below.

1. (Original) A system, comprising:

a plurality of processors, each comprising at least one arithmetic logic unit, an instruction processing unit, and a plurality of processor ports; and

a plurality of dynamically configurable communication elements, each comprising a plurality of communication ports, a first memory, and a routing engine;

wherein said plurality of processors and said plurality of dynamically configurable communication elements are coupled together in an interspersed arrangement;

wherein, for each of said processors, said plurality of processor ports are configured for coupling to a first subset of said plurality of dynamically configurable communication elements;

wherein, for each of said dynamically configurable communication elements, said plurality of communication ports comprise a first subset of communication ports configured for coupling to a subset of said plurality of said processors and a second subset of communication ports configured for coupling to a second subset of said plurality of dynamically configurable communication elements.

2. (Original) The system as recited in claim 1,

wherein each of said processors is coupled to each of a plurality of neighboring dynamically configurable communication elements via a respective one of said plurality of processor ports;

wherein each of said dynamically configurable communication elements is coupled to a plurality of neighboring processors via a respective one of said first subset of said plurality of communication ports;

wherein each of said dynamically configurable communication elements is coupled to each of a plurality of neighboring dynamically configurable communication

elements via a respective one of said second subset of said plurality of communication ports.

3. (Original) The system as recited in claim 1,

wherein each of said processors is coupled to each of four neighboring dynamically configurable communication elements via a respective one of said plurality of processor ports;

wherein each of said dynamically configurable communication elements is coupled to each of four neighboring processors via a respective one of said first subset of said plurality of communication ports;

wherein each of said dynamically configurable communication elements is coupled to each of four neighboring dynamically configurable communication elements via a respective one of said second subset of said plurality of communication ports.

4. (Original) The system as recited in claim 1, wherein said plurality of processors and said plurality of dynamically configurable communication elements are interspersed in a substantially homogeneous fashion.

5. (Original) The system as recited in claim 1,

wherein, for each of said processors, said instruction processing unit is coupled to control said at least one arithmetic logic unit;

wherein each of said processors further comprises at least a second memory including a plurality of addressable locations, wherein said second memory is coupled to said at least one instruction processing unit; and

wherein, for each of said processors, said plurality of processor ports comprise a first subset of processor ports coupled to said at least one arithmetic logic unit and a second subset of processor ports coupled to said instruction processing unit.

6. (Original) The system as recited in claim 1,

wherein, for each of said dynamically configurable communication elements, said first memory is shared among a plurality of said processors.

7. (Original) The system as recited in claim 1,

wherein, for each of said dynamically configurable communication elements, said first memory is shared among a plurality of neighboring processors.

8. (Original) The system as recited in claim 1,

wherein, for each of said dynamically configurable communication elements, said first memory is shared among four neighboring processors.

9. (Original) The system as recited in claim 1,

wherein, for each of said dynamically configurable communication elements, said first memory operates as at least a portion of a register file for its neighboring processors.

10. (Original) The system as recited in claim 1, wherein each of said processors is dynamically configurable to obtain data from the first memory of different ones of said dynamically configurable communication elements.

11. (Original) The system as recited in claim 1,

wherein, for each of said dynamically configurable communication elements, said first memory stores data that is directly accessible by a processor during execution of instructions.

12. (Original) The system as recited in claim 1,

wherein, for each of said dynamically configurable communication elements, said first memory stores data that is directly accessible by each of a plurality of neighboring processors during execution of instructions.

13. (Original) The system as recited in claim 1,

wherein each of the processors is operable to obtain data from a first memory of any of a plurality of neighboring dynamically configurable communication elements.

14. (Original) The system as recited in claim 1,

wherein a first processor is operable to obtain first data from a first memory of a first dynamically configurable communication element during a first time period, and wherein the first processor is operable to obtain second data from a first memory of a second dynamically configurable communication element during a second time period.

15. (Original) The system as recited in claim 1,

wherein a first processor is operable to obtain a plurality of data values from a respective subset of said plurality of dynamically configurable communication elements substantially simultaneously.

16. (Original) The system as recited in claim 1,

wherein, for each of said dynamically configurable communication elements, said first memory is configured to provide a plurality of data values to a respective subset of said plurality of processors substantially simultaneously.

17. (Original) The system as recited in claim 1,

wherein, for each of said dynamically configurable communication elements, the first memory is coupled to said plurality of communication ports via a plurality of access ports and includes a plurality of addressable locations; and

wherein, for each of said dynamically configurable communication elements, said routing engine is coupled to said plurality of communication ports and configured to route data between any of said plurality of communication ports.

18. (Original) The system as recited in claim 1, wherein each of said plurality of dynamically configurable communication elements further comprises a direct memory access engine coupled to said plurality of communication ports and configured to transfer data between the first memory and said plurality of communication ports.

19. (Original) The system as recited in claim 1,

wherein different pathways are operable to be created for data transfer among different subsets of said dynamically configurable communication elements;

20. (Original) The system as recited in claim 19,

wherein each of at least a subset of the processors is operable to dynamically create different pathways for data transfer among different subsets of said dynamically configurable communication elements.

21. (Original) The system as recited in claim 19,

wherein each of at least a subset of the dynamically configurable communication elements is operable to dynamically create pathways among different subsets of said dynamically configurable communication elements.

22. (Original) The system as recited in claim 19,

wherein a first pathway comprises a first plurality of dynamically configurable communication elements;

wherein, for each of the first plurality of dynamically configurable communication elements in the first pathway, the first pathway is dynamically created by configuring the routing engine of the dynamically configurable communication element to implement a portion of the first pathway prior to initiating a data transfer.

23. (Original) The system as recited in claim 19, wherein a given pathway is dynamically created via, for each of said subset of said dynamically configurable communication elements, configuring said routing engine to implement said pathway in response to receiving a first portion of a data transfer, wherein said first portion includes routing information.

24. (Original) The system as recited in claim 19, wherein each pathway is operable to be destroyed, wherein a given pathway remains available for data transfer until destroyed.

25. (Original) The system as recited in claim 19,

wherein a respective pathway is operable to remain available regardless of any transfer of message data on the respective pathway.

26. (Original) The system as recited in claim 19,

wherein a first processor is operable to configure a first dynamically configurable communication element to provide data directly to a neighboring second dynamically configurable communication element;

wherein the first processor is operable to create a pathway between the first dynamically configurable communication element and a remote third dynamically configurable communication element to enable the first dynamically configurable communication element to provide data through the pathway to the remote third dynamically configurable communication element.

27. (Original) The system as recited in claim 1,

wherein one of said processors is configurable as a source device to transfer a first plurality of data through an intermediate subset of said plurality of dynamically configurable communication elements to a destination device;

wherein, after said source device begins transfer of said first plurality of data through said intermediate subset to said destination device, if either said destination device or one of said intermediate subset stalls, the stalling device is operable to propagate stalling information through one or more of said intermediate subset to said source device;

wherein said source device is operable to suspend transfer of said first plurality of data upon receipt of the stalling information, wherein a portion of said first plurality of data transmitted after said stalling and prior to the suspending is buffered in at least one of said intermediate subset.

28. (Original) The system as recited in claim 27,

wherein, if said stalling device becomes available for communication, said stalling device is operable to propagate communication availability information through one or more of said intermediate subset to said source device;

wherein said at least one of said intermediate subset transmits said portion of said first plurality of data to said destination device after said stalling device becomes available for communication;

wherein said source device resumes transfer of said first plurality of data upon receipt of said communication availability information.

29. (Original) The system as recited in claim 28,

wherein said first plurality of data is conveyed via a plurality of data signals;

wherein said stalling information is conveyed via assertion of a blocked signal;

wherein said communication availability information is conveyed via de-assertion of a blocked signal; and

wherein said blocked signal is routed parallel to said plurality of data signals.

30. (Original) The system as recited in claim 1,

wherein one of said processors is configurable as a source device to transfer a first plurality of data through an intermediate subset of said plurality of dynamically configurable communication elements to a destination device;

wherein, after said source device begins transfer of said first plurality of data through said intermediate subset to said destination device, if either said source device or one of said intermediate subset stalls, the stalling device is operable to propagate stalling information through one or more of said intermediate subset to said destination device;

wherein said destination device is operable to suspend processing of said first plurality of data upon receipt of the stalling information.

31. (Original) The system as recited in claim 30,

wherein, if said stalling device becomes available for communication, said stalling device is operable to propagate communication availability information through one or more of said intermediate subset to said destination device;

wherein said destination device resumes processing of said first plurality of data upon receipt of said communication availability information.

32. (Original) The system as recited in claim 31,

wherein said first plurality of data is conveyed via a plurality of data signals;

wherein said stalling information is conveyed via assertion of an idle signal;

wherein said communication availability information is conveyed via de-assertion of said idle signal; and

wherein said idle signal is routed in parallel with said plurality of data signals.

33. (Original) The system as recited in claim 1,

wherein one of said processors is configurable as a source device to transfer a first plurality of data through an intermediate subset of said plurality of dynamically configurable communication elements to a destination device;

wherein, after said source device begins transfer of said first plurality of data through said intermediate subset to said destination device, if one of said source device, one of said intermediate subset, or said destination device stalls, the stalling device is operable to propagate stalling information through one or more of said intermediate subset to one or more of said source device and said destination device;

wherein said source device is operable to suspend transfer of said first plurality of data upon receipt of said stalling information, wherein a portion of said first plurality of data transmitted after said stalling and prior to the suspending is buffered in at least one of said intermediate subset;

wherein said destination device is operable to suspend processing of said first plurality of data upon receipt of said stalling information.

34. (Original) The system as recited in claim 33,

wherein, if said stalling device becomes available for communication, said stalling device is operable to propagate communication availability information through one or more of said intermediate subset to one or more of said source device and said destination device;

wherein said at least one of said intermediate subset transmits said portion of said first plurality of data to said destination device after said stalling device becomes available for communication;

wherein said source device resumes transfer of said first plurality of data upon receipt of said communication availability information;

wherein said destination device resumes processing of said first plurality of data upon receipt of said communication availability information.

35. (Original) The system as recited in claim 34,

wherein said first plurality of data is conveyed via a plurality of data signals;

wherein said stalling information is conveyed via a blocked signal and an idle signal;

wherein said blocked signal and said idle signal are routed parallel to said plurality of data signals.

36. (Original) The system as recited in claim 1, wherein each of said dynamically configurable communication elements further comprises:

a plurality of input ports;

a plurality of output registers;

a crossbar coupled to receive data from one or more of said plurality of input ports and to transmit data to a selected one or more of said plurality of output registers;

wherein each said output register selectively operates in a synchronous data transfer mode or a transparent data transfer mode.

37. (Original) The system as recited in claim 1, wherein said plurality of processors and said plurality of dynamically configurable communication elements are manufactured on a single integrated circuit.

38. (Original) The system as recited in claim 1,

wherein each of at least a subset of the processors is operable to be enabled / disabled as needed to reduce power consumption

39. (Original) The system as recited in claim 1,

wherein each of at least a subset of the processors is operable to operate in a synchronous fashion.

40. (Original) The system as recited in claim 1,

wherein the first memory of each of the dynamically configurable communication elements comprises only an accumulator, a status register, operand buffers, and one or more address generator controls.

41. (Original) A system, comprising:

a plurality of processors;

a plurality of dynamically configurable communication elements, each comprising a plurality of communication ports, a first memory, and a routing engine;

wherein the plurality of processors and the plurality of dynamically configurable communication elements are coupled together in an interspersed arrangement;

wherein one of said processors is configurable as a source device to transfer a first plurality of data through an intermediate subset of said plurality of dynamically configurable communication elements to a destination device;

wherein, after said source device begins transfer of said first plurality of data through said intermediate subset to said destination device, if either said destination device or one of said intermediate subset stalls, the stalling device is operable to propagate stalling information through one or more of said intermediate subset to said source device;

wherein said source device is operable to suspend transfer of said first plurality of data upon receipt of the stalling information, wherein a portion of said first plurality of data transmitted after said stalling and prior to the suspending is buffered in at least one of said intermediate subset.

42. (Original) The system as recited in claim 41,

wherein, if said stalling device becomes available for communication, said stalling device is operable to propagate communication availability information through one or more of said intermediate subset to said source device;

wherein said at least one of said intermediate subset transmits said portion of said first plurality of data to said destination device after said stalling device becomes available for communication;

wherein said source device resumes transfer of said first plurality of data upon receipt of said communication availability information.

43. (Original) A system, comprising:

a plurality of processors;

a plurality of dynamically configurable communication elements, each comprising a plurality of communication ports, a first memory, and a routing engine;

wherein the plurality of processors and the plurality of dynamically configurable communication elements are coupled together in an interspersed arrangement;

wherein one of said processors is configurable as a source device to transfer a first plurality of data through an intermediate subset of said plurality of dynamically configurable communication elements to a destination device;

wherein, after said source device begins transfer of said first plurality of data through said intermediate subset to said destination device, if either said source device or one of said intermediate subset stalls, the stalling device is operable to propagate stalling information through one or more of said intermediate subset to said destination device;

wherein said destination device is operable to suspend processing of said first plurality of data upon receipt of the stalling information.

44. (Original) The system as recited in claim 43,

wherein, if said stalling device becomes available for communication, said stalling device is operable to propagate communication availability information through one or more of said intermediate subset to said destination device;

wherein said destination device resumes processing of said first plurality of data upon receipt of said communication availability information.

45. (Original) A method for transferring data from a source device to a destination device, wherein said source device is coupled to said destination device through a plurality of intermediate devices, the method comprising:

configuring said source device to transfer a first plurality of data to said destination device through said plurality of intermediate devices;

said source device beginning transfer of said first plurality of data through said plurality of intermediate devices to said destination device;

at least one of said intermediate devices or said destination device stalling after said beginning transfer;

propagating stalling information through one or more of said intermediate devices to said source device after said stalling;

said source device suspending transfer of said first plurality of data upon receipt of said stalling information, wherein a subset of said first plurality of data transmitted after said stalling and prior to said suspending is buffered in one or more of said intermediate devices.

46. (Original) The method as recited in claim 45, further comprising:

said at least one of said intermediate devices or said destination device becoming available for communication;

propagating communication availability information to said source device after said becoming available;

the subset of said intermediate devices transmitting the subset of said first plurality of data to said destination device after said becoming available;

said source device resuming transfer of said first plurality of data upon receipt of said communication availability information.

47. (Original) The method as recited in claim 45, wherein the method operates in a system comprising a plurality of processors and a plurality of dynamically configurable communication elements;

wherein said plurality of processors and said plurality of dynamically configurable communication elements are manufactured on a single integrated circuit;

wherein said plurality of processors and said plurality of dynamically configurable communication elements are coupled together in an interspersed arrangement;

wherein said source device comprises one of said processors;

wherein said plurality of intermediate devices comprise a plurality of dynamically configurable communication elements.

48. (Original) The method as recited in claim 47,

wherein each of said plurality of processors comprises at least one arithmetic logic unit, at least one instruction processing unit, and a plurality of processor ports;

wherein each of said plurality of dynamically configurable communication elements comprises a plurality of communication ports, at least one memory, and a routing engine.

49. (Original) A method for transferring data from a source device to a destination device, wherein said source device is coupled to said destination device through a plurality of intermediate devices, the method comprising:

configuring said source device to transfer a first plurality of data to said destination device through said plurality of intermediate devices;

said source device beginning transfer of said first plurality of data through said plurality of intermediate devices to said destination device;

at least one of said intermediate devices or said source device stalling after said beginning transfer;

propagating stalling information through one or more of said intermediate devices to said destination device after said stalling; and

said destination device suspending processing of said first plurality of data upon receipt of said stalling information.

50. (Original) The method as recited in claim 49, further comprising:

said at least one of said intermediate devices or said source device becoming available for communication;

propagating communication availability information to said destination device after said becoming available;

said destination device resuming processing of said first plurality of data upon receipt of said communication availability information.

51. (Original) The method as recited in claim 49, wherein the method operates in a system comprising a plurality of processors and a plurality of dynamically configurable communication elements;

wherein said plurality of processors and said plurality of dynamically configurable communication elements are manufactured on a single integrated circuit;

wherein said plurality of processors and said plurality of dynamically configurable communication elements are coupled together in an interspersed arrangement;

wherein said source device comprises one of said processors;

wherein said plurality of intermediate devices comprise a plurality of dynamically configurable communication elements.

52. (Original) A system, comprising:

a plurality of processors, each comprising at least one arithmetic logic unit, at least one instruction processing unit, and a plurality of processor ports;

a plurality of dynamically configurable communication elements, each comprising a plurality of communication ports, at least a first memory, and a routing engine;

wherein said plurality of processors and said plurality of dynamically configurable communication elements are manufactured on a single integrated circuit;

wherein the plurality of processors and the plurality of dynamically configurable communication elements are coupled together in an interspersed arrangement;

wherein each of said dynamically configurable communication elements comprises:

a plurality of input ports;

a plurality of output registers;

a crossbar coupled to receive data from one or more of said plurality of input ports and to transmit data to a selected one or more of said plurality of output registers;

wherein each said output register selectively operates in a synchronous data transfer mode or a transparent data transfer mode.

53. (Original) The system as recited in claim 52,

wherein, for each of said processors, said at least one instruction processing unit is coupled to control said at least one arithmetic logic unit;

wherein each of said processors further comprises at least a second memory including a plurality of addressable locations, wherein said second memory is coupled to said at least one instruction processing unit; and

wherein the plurality of processor ports comprise a first subset of processor ports coupled to said at least one arithmetic logic unit and a second subset of processor ports coupled to said at least one instruction processing unit.

54. (Original) The system as recited in claim 52,

wherein said plurality of communication ports comprise a first subset of communication ports configured for coupling to a subset of said plurality of processors and a second subset of communication ports configured for coupling to a subset of said plurality of dynamically configurable communication elements;

wherein said at least a first memory is coupled to said plurality of communication ports via a plurality of access ports and includes a plurality of addressable locations; and

wherein said routing engine is coupled to said plurality of communication ports and configured to route data between any of said plurality of communication ports.

55. (Original) The system as recited in claim 52, wherein each of said plurality of dynamically configurable communication elements further comprises a direct memory access engine coupled to said plurality of communication ports and configured to transfer data between said at least a first memory and said plurality of communication ports.

56. (Original) A system, comprising:

an interconnect network; and

a plurality of dynamically configurable communication elements configured to exchange data, each said element comprising:

a plurality of input ports coupled to said interconnect network;

a plurality of output registers coupled to said interconnect network;

a crossbar coupled to receive data from one or more of said plurality of input ports and to transmit data to a selected one or more of said plurality of output registers;

wherein each said output register selectively operates in a synchronous data transfer mode or a transparent data transfer mode.

57. (Original) A method for transferring data from a source device to a destination device, wherein said source device is coupled to said destination device through a plurality of intermediate devices, the method comprising:

configuring said source device to transfer a first plurality of data to said destination device through said plurality of intermediate devices;

configuring each of said plurality of intermediate devices to operate in a synchronous data transfer mode or a transparent data transfer mode;

transferring said first plurality of data through a single intermediate device during a single master clock cycle dependent upon said single intermediate device being configured to operate in a synchronous data transfer mode; and

transferring said first plurality of data through multiple intermediate devices during a single master clock cycle dependent upon each of said multiple intermediate devices being configured to operate in a transparent data transfer mode.

58. (Original) The method as recited in claim 57,

wherein the method operates in a system comprising a plurality of processors and a plurality of dynamically configurable communication elements;

wherein said plurality of processors and said plurality of dynamically configurable communication elements are coupled together in an interspersed arrangement;

wherein said plurality of processors and said plurality of dynamically configurable communication elements are manufactured on a single integrated circuit.

59. (Original) The method as recited in claim 58,

wherein said source device comprises one of said processors;

wherein said plurality of intermediate devices comprise a plurality of dynamically configurable communication elements;

60. (Original) The method as recited in claim 58,

wherein each of said plurality of processors comprises at least one arithmetic logic unit, at least one instruction processing unit, and a plurality of processor ports;

wherein each of said plurality of dynamically configurable communication elements comprises a plurality of communication ports, at least one memory, and a routing engine.

61. (Original) A method for transferring data from a source device to a plurality of destination devices, wherein said source device is coupled to each of said destination devices through a plurality of intermediate devices, the method comprising:

configuring said source device to transfer a first plurality of data to a first destination device through one or more intermediate devices;

configuring each of said plurality of intermediate devices to operate in a synchronous data transfer mode;

transferring said first plurality of data from said source device to said first destination device during a first time period, wherein said first time period comprises one

or more master clock cycles, and wherein said transferring comprises transferring the first plurality of data through a single intermediate device during each said master clock cycle;

configuring said source device to transfer a second plurality of data to a second destination device through said plurality of intermediate devices;

configuring each of said plurality of intermediate devices to operate in a transparent data transfer mode;

transferring said second plurality of data from said source device to said second destination device through multiple intermediate devices during a single master clock cycle.

62. (Original) A method of manufacturing an integrated circuit, the method comprising:

fabricating a unit comprising a processor and a dynamically configurable communication element;

wherein the processor comprises an arithmetic logic unit, an instruction processing unit, and a plurality of processor ports;

wherein the dynamically configurable communication element comprises a plurality of communication ports, a first memory, and a routing engine;

placing and interconnecting a plurality of said units on a substrate, wherein said plurality of processors and said plurality of dynamically configurable communication elements are coupled together in an interspersed arrangement;

wherein, for each of said processors, said plurality of processor ports are configured for coupling to a first subset of said plurality of dynamically configurable communication elements;

wherein, for each of said dynamically configurable communication elements, said plurality of communication ports comprise a first subset of communication ports configured for coupling to a subset of said plurality of processors and a second subset of communication ports configured for coupling to a second subset of said plurality of dynamically configurable communication elements.

63. (Original) A system, comprising:

a plurality of processors, each comprising:

at least one arithmetic logic unit;

at least one instruction processing unit coupled to control said arithmetic logic unit and including at least a first memory including a plurality of addressable locations; and

a plurality of processor ports, including a first subset coupled to said arithmetic logic unit and a second subset coupled to said instruction processing unit;

a plurality of dynamically configurable communication elements, each comprising:

a plurality of communication ports, including a third subset configured for coupling to a subset of said plurality of processors and a fourth subset configured for coupling to a subset of said plurality of dynamically configurable communication elements;

at least a second memory coupled to said plurality of communication ports via a plurality of access ports and including a plurality of addressable locations;

a routing engine coupled to said plurality of communication ports and configured to route data between any of said plurality of communication ports; and

a direct memory access engine coupled to said plurality of communication ports and configured to transfer data between said second memory and said plurality of communication ports;

wherein said plurality of processors and said plurality of dynamically configurable communication elements are manufactured on a single integrated circuit.

64. (New) The system as recited in claim 1, wherein for at least one of said dynamically configurable communication elements, said first memory includes a plurality of addressable locations and is configured to substantially simultaneously provide a

plurality of values stored in said plurality of addressable locations to two or more of said processors.